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AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1-14. (Canceled).

15. (Currently Amended) A method of manufacture of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of columnar laminates having, at an upper portion and a lower portion thereof, a first semiconductor region and a second semiconductor region, respectively, while spacing the plurality of columnar laminates in a first direction and in a second direction wider than the first direction;

(b) forming conductive films over the side walls of the columnar laminates via a first insulating film with a distance, in the first direction, between the conductive films over the side walls of the plurality of columnar laminates as a first distance and with a distance in the second direction as a second distance which is greater than the first distance;

(c) forming a second insulating film to a thickness sufficient to fill a space of the first distance and but not sufficient to fill a space of the second distance; and

(d) forming a third insulating film over the second insulating film and filling the space of the second distance

(e) etching the second and third insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is exposed; and

(f) etching the conductive film exposed by the step (e).

16. (Currently Amended) A method of manufacture of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of columnar laminates having, at an upper portion and a lower portion thereof, a first semiconductor region and a second semiconductor region, respectively, while spacing the plurality of columnar laminates in a first direction and in a second direction wider than the first direction;

(b) forming conductive films over the side walls of the columnar laminates via a first insulating film with a distance, in the first direction, between the conductive films over the side walls of the plurality of columnar laminates as a first distance and with a distance in the second direction as a second distance which is greater than the first distance;

(c) depositing a second insulating film between the columnar laminates and thereover with a thickness at least equal to the first distance; and

(d) depositing over the second insulating film a third insulating film with a thickness corresponding to at least 70% of a vertical difference, after the step (c), between the top of the second insulating film over the second distance portion of the columnar laminates and the top of the second insulating film over the columnar laminates

(e) etching the second and third insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is exposed; and

(f) etching the conductive film exposed by the step (e).

17. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the step (c) is carried out at a temperature of 700°C or less.

18. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the step (c) and the step (d) are carried out at a temperature of 700°C or less.

19. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, further comprising, after the step (d), the steps of:

(e) depositing a fourth insulating film over the third insulating film; and

(f) etching the second, third and fourth insulating films until the conductive film existing over the side walls of the first semiconductor region of the columnar laminate is exposed.

20. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 19, further comprising, after the step (g), a step of:

(h) forming a fifth insulating film over the second and third insulating films.

21. (Canceled).

22. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 21, further comprising, after the step (f), a step of:

(g) forming a fourth insulating film over the second and third insulating films.

23. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the second insulating film has better coverage than the third insulating film.

24. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the second insulating film is a silicon oxide film and the step (c) is carried out by chemical vapor deposition using tetraethoxysilane as a raw material.

25. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the second insulating film is a silicon oxide film and the step (c) is carried out by chemical vapor deposition using tetraethoxysilane and ozone (O_3) as raw materials.

26. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the third insulating film is a silicon oxide film and the step (d) is carried out in a plasma atmosphere having a plasma density of $10^{11}/cm^2$ or greater.

27. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the columnar laminate has a height of at least 3 times as much as the first distance.

28. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the first distance is 150 nm or less and the second distance is 500 nm or greater.

29. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the plane pattern of each of the columnar laminate and the conductive film over the side walls thereof is approximately elliptical and a first diameter in the first direction is smaller than a second diameter in the second direction.

30. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the columnar laminate in the step (a) is formed using a mask which is H-shaped in the first direction.

31. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, further comprising, prior to the step (a), the steps of:

(h) forming two pairs of horizontal MISFETs having source and drain regions in common; and

(i) connecting the second semiconductor regions of the two vertical MISFETs adjacent to each other in the first direction to the source and drain regions which the two pairs of horizontal MISFETs have in common, respectively.

32. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, further comprising, prior to the step (a), the steps of:

(j) forming two horizontal MISFETs; and

(k) connecting the second semiconductor regions of the two vertical MISFETs that are adjacent to each other in the first direction to one of the ends of the two horizontal MISFETs, respectively.

33-41. (Canceled).

42. (Previously Presented) A method of manufacture of a semiconductor integrated circuit device according to claim 15, wherein the conductive films are formed to encompass the columnar laminates.

43. (New) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first columnar laminate, a second columnar laminate and a third columnar laminate over a semiconductor substrate;

(b) forming first insulating films over side walls of the first, the second and the third columnar laminates;

(c) forming conductive films over the side walls of the first, the second and the third columnar laminates via the first insulating films;

(d) forming a second insulating film to cover the conductive films, the first columnar laminate, the second columnar laminate and the third columnar laminate; and

(e) forming a third insulating film over the second insulating film;

wherein the second columnar laminate is adjusted to the first columnar laminate in a first direction,

wherein the third columnar laminate is adjusted to the first columnar laminate in a second direction being perpendicular to the first direction,

wherein a second distance between the first columnar laminate and the third columnar laminate is wider than a first distance between the first columnar laminate and the second columnar laminate,

wherein the second insulating film has a thickness enough to fill a space of the first distance and but not enough to fill a space of the second distance, and

wherein the third insulating film has a thickness enough to fill a space of the second distance.

44. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 43, further comprising the steps of:

(g) before the step (a), forming a MISFET on the semiconductor substrate.

45. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 43,

wherein the second insulating film is comprised of a silicon oxide film and the step (d) is carried out by chemical vapor deposition using tetraethoxysilane as a raw material.

46. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 43,

wherein the second insulating film is comprised of a silicon oxide film and the step (d) is carried out by chemical vapor deposition using tetraethoxysilane and ozone (O3) as raw materials.

47. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 43,

wherein the third insulating film is comprised of a silicon oxide film and the step (f) is carried out in a plasma atmosphere having a plasma density of 101/cm2 or greater.

48. (New) A manufacturing method of a semiconductor integrated circuit device according to claim 43,

wherein the first distance is 150 nm or less and the second distance is 500 nm or greater.